CLAIMS

1.   A method of jitter compensation of a phase locked loop frequency synthesizer by means of a variable delay, the method c h a r a c t e r i z e d   i n that the jitter is compensated prior to a signal being subject to jitter is

5   passed through a non-linearity, the jitter compensating variable delay being realized by means of a tapped delay line.

2.   The method according to claim 1 c h a r a c t e r - i z e d   i n that each of a plurality of integer divisors

10   are selected according to a fractional pattern, represent- ing fractional weighting of the integer divisors, generated by a $\Sigma\Delta$ modulator from a fractional setting input.

3.   The method according to claim 1 or 2 c h a r a c - t e r i z e d   i n that a fraction of a first and a second

15   integer is determined by a binary fractional pattern, for selecting the first or the second integer, generated by a $\Sigma\Delta$ modulator from a fractional setting input.

4.   The method according to claim 2 or 3 c h a r a c - t e r i z e d   i n that the tapped delay line is con-

20   trolled by means of control signals derived from the $\Sigma\Delta$ modulator.

5.   The method according to claim 4 c h a r a c t e r - i z e d   i n that a control signal for controlling the tapped delay line is determined by integrating and scaling

25   an error signal being the difference between a signal rep- resenting the fraction and a signal carrying the fractional pattern.

6.   The method according to any of claims 1-5 c h a r - a c t e r i z e d   i n   that the tapped delay line com-

prises a plurality of capacitors with capacitances propor-
tional to successive powers of 2.

7.   The method according to claim 5 or 6   c h a r a c -
t e r i z e d   i n   that the control signal carries a bi-
5   nary number whose bit representation connects or discon-
nects capacitors of the tapped delay line with respective
capacitances corresponding to bit positions of the binary
representation.

8.   The method according to any of claims 1-5   c h a r -
10   a c t e r i z e d   i n   that the tapped delay line com-
prises a plurality of serially connected delay elements.

9..   The method according to claim 5 or 8   c h a r a c -
t e r i z e d   i n   that the control signal carries a rep-
resentation for connecting or disconnecting a delay element
15   of the tapped delay line to either the input or output of
the tapped delay line.

10.   The method according to claim 9   c h a r a c t e r -
i z e d   i n   that the control signal carries a bit repre-
sentation for connecting or disconnecting a delay element
20   output to the output of the tapped delay line.

11.   The method according to claim 9   c h a r a c t e r -
i z e d   i n   that the control signal carries a bit repre-
sentation for connecting or disconnecting a delay element
input to the input of the tapped delay line.

25   12.   The method according to any of claims 1-11   c h a r -
a c t e r i z e d   i n   that the non-linearity is included
in or is a phase or frequency detector.

13.   The method according to any of claims 1-12   c h a r -
a c t e r i z e d   i n   that the output signal of the

tapped delay line is input to the phase or frequency detector.

14. The method according to any of claims 1-13 c h a r - a c t e r i z e d i n that at least one of

5   - a reference frequency signal,

           - a frequency divided output signal of a voltage controlled oscillator,

           - a frequency divided output signal of the frequency synthesizer,

10   is input to and delayed by the tapped delay line.

15. The method according to any of claims 1-12 c h a r - a c t e r i z e d i n that the output signal of the tapped delay line is input to frequency dividing circuitry.

16. The method according to any of claims 1-12 and 15
15   c h a r a c t e r i z e d i n that at least one of

           - an output signal of a voltage controlled oscillator, and

           - an output signal of the frequency synthesizer

is input to and delayed by the tapped delay line.

20   17. A phase locked loop frequency synthesizer with jitter compensation by means of a variable delay, the frequency synthesizer c h a r a c t e r i z e d b y a tapped delay line compensating the jitter prior to a signal being subject to jitter is passed through a non-linearity.

25   18. The frequency synthesizer according to claim 17 c h a r a c t e r i z e d b y a $\Sigma\Delta$ modulator for generating or a storing element for pre-generated storing of a fractional pattern representing fractional weighting of a

plurality of integer divisors, the fractional pattern se-
lecting one integer divisor, out of the plurality of inte-
ger divisors, at a time to be active.

19. The frequency synthesizer according to claim 17 or 18
c h a r a c t e r i z e d   b y   a $\Sigma\Delta$ modulator for generat-
ing or a storing element for pre-generated storing of a bi-
nary fractional pattern for determining a fraction of a
first and a second integer, the binary fractional pattern
selecting the first or the second integer, the binary frac-
tional pattern being generated from or restored from a
fractional setting input.

20. The frequency synthesizer according to claim 19
c h a r a c t e r i z e d   b y   control means for control-
ling the tapped delay line by means of one or more control
signals derived from the $\Sigma\Delta$ modulator.

21. The frequency synthesizer according to claim 20
c h a r a c t e r i z e d   b y   an integrator integrating
and scaling an error signal being the difference between a
signal representing the fraction and a signal carrying the
binary fractional pattern, the integrator output signal be-
ing a signal for controlling the tapped delay line.

22. The frequency synthesizer according to any of claims
17-21 c h a r a c t e r i z e d   i n   that the tapped de-
lay line comprises a plurality of capacitors with capaci-
tances proportional to successive powers of 2.

23. The frequency synthesizer according to claim 21 or 22
c h a r a c t e r i z e d   b y   switches for connecting or
disconnecting capacitors of the tapped delay line, wherein
respective capacitances corresponding to bit positions of a
binary representation of a binary number are connected or

disconnected, the binary number being carried by the one or more control signals.

24. The frequency synthesizer according to any of claims 17-21 c h a r a c t e r i z e d   b y   the tapped delay line comprising a plurality of serially connected delay elements.

25. The frequency synthesizer according to claim 21 or 24 c h a r a c t e r i z e d   b y   one or more switches for connecting or disconnecting one or more delay elements to the input or output of the tapped delay line according to a bit representation, the bit representation being carried by a control signal.

26. The frequency synthesizer according to claim 25 c h a r a c t e r i z e d   b y   the one or more switches each connecting or disconnecting a delay element output to the output of the tapped delay line.

27. The frequency synthesizer according to claim 25 c h a r a c t e r i z e d   b y   the one or more switches each connecting or disconnecting a delay element input to the input of the tapped delay line.

28. The frequency synthesizer according to any of claims 17-27 c h a r a c t e r i z e d   i n   that the non-linearity is included in or is a phase or frequency detector.

29. The frequency synthesizer according to any of claims 17-28 c h a r a c t e r i z e d   i n   that the output signal of the tapped delay line is input to the phase or frequency detector.

30. The frequency synthesizer according to any of claims 17-29 c h a r a c t e r i z e d   i n   that at least one of

    - a reference frequency signal,

- a frequency divided output signal of a voltage
  controlled oscillator,

- a frequency divided output signal of the fre-
  quency synthesizer,

5   is input to and delayed by the tapped delay line.

31. The frequency synthesizer according to any of claims
17-28 c h a r a c t e r i z e d   i n that the output sig-
nal of the tapped delay line is input to frequency dividing
circuitry.

10 32. The frequency synthesizer according to any of claims
17-28 and 31 c h a r a c t e r i z e d   i n that at least
one of

          - an output signal of a voltage controlled oscil-
            lator, and

15   - an output signal of the frequency synthesizer

is input to and delayed by the tapped delay line.

33. A radio communications system c h a r a c t e r -
i z e d   b y means for carrying out the method in any of
claims 1-16.

20 34. A radio communications system c h a r a c t e r -
i z e d   b y one or more frequency synthesizers according
to any of claims 17-32.